CLAIMS

I Claim:

1. A programmable logic device (PLD) comprising:

programmable logic that includes test logic;

a port for external communication;

a hard-coded microprocessor in communication with said programmable logic; and

memory that includes a test routine, said memory being in communication with said microprocessor and said programmable logic, whereby said test logic is tested using said test routine under control of said microprocessor.

2. A PLD as recited in claim 1 wherein said port is a parallel port, a serial port, a USB port or a JTAG port.

3. A PLD as recited in claim 1 wherein said memory is part of said programmable logic.

4. A PLD as recited in claim 1 wherein said memory is part of said microprocessor.

5. A PLD as recited in claim 1 wherein said microprocessor includes an analysis routine for analyzing results of said test routine.

6. A PLD as recited in claim 1 wherein said microprocessor includes a control routine for controlling execution of said test routine.

7. A programmable logic device (PLD) comprising:

programmable logic that includes user logic;

a port for external communication;

a hard-coded microprocessor in communication with said programmable logic; and

memory that includes a debugging routine, said memory being in communication with said microprocessor and said programmable logic, whereby said user logic is debugged using said debugging routine under control of said microprocessor.

8. A PLD as recited in claim 7 wherein said port is a parallel port, a serial port, a USB port or a JTAG port.

9. A PLD as recited in claim 7 wherein said memory is part of said programmable logic.

10. A PLD as recited in claim 7 wherein said memory is part of said microprocessor.

11. A PLD as recited in claim 7 wherein said microprocessor includes an analysis routine for analyzing results of said debugging routine.

12. A PLD as recited in claim 7 wherein said microprocessor includes a control routine for controlling execution of said debugging routine.

13. A method of testing a programmable logic device (PLD), said method comprising:

manufacturing a PLD that includes programmable logic, an embedded microprocessor and associated memory;

downloading to said memory a test routine;

executing said test routine under control of said microprocessor to test said programmable logic;

storing raw data resulting from execution of said test routine; and

sending results based on said raw data of said test routine from said microprocessor to a test system external to said PLD, whereby said test system determines the functionality of said PLD.

14. A method as recited in claim 13 further comprising:

downloading to said microprocessor a control routine for controlling execution of said test routine.

15. A method as recited in claim 13 wherein said results are said raw data.

16. A method as recited in claim 13 further comprising:

downloading to said microprocessor an analysis routine for analyzing said raw data from said test routine; and

executing said analysis routine to produce said results, wherein said results reflect conclusions based on said raw data.

17. A method as recited in claim 13 further comprising:

downloading to said microprocessor a compression routine for compressing said raw data from said test routine;

compressing said raw data; and

sending said compressed raw data as said results.

18. A method as recited in claim 13 wherein said associated memory is part of said programmable logic.

19. A method as recited in claim 13 wherein said associated memory is part of said microprocessor.

20. A method of debugging a programmable logic device (PLD), said method comprising:

mounting in a test socket a PLD that includes user logic, an embedded microprocessor and associated memory;

downloading to said memory a debugging routine;

executing said debugging routine under control of said microprocessor to debug said user logic;

storing raw data resulting from execution of said debugging routine; and

sending results based on said raw data of said debug routine from said microprocessor to a host computer external to said PLD, whereby said host computer determines the functionality of said PLD.

21. A method as recited in claim 20 further comprising:

downloading to said microprocessor a control routine for controlling execution of said debugging routine.

22. A method as recited in claim 20 wherein said results are said raw data.

23. A method as recited in claim 20 further comprising:

downloading to said microprocessor an analysis routine for analyzing said raw data from said debugging routine; and

executing said analysis routine to produce said results, wherein said results reflect conclusions based on said raw data.

24. A method as recited in claim 20 further comprising:

downloading to said microprocessor a compression routine for compressing said raw data from said debugging routine;

compressing said raw data; and

sending said compressed raw data as said results.

25. A method as recited in claim 20 wherein said associated memory is part of said user logic.

26. A method as recited in claim 20 wherein said associated memory is part of said microprocessor.